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(32 AND 1).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	4
(L32 AND L1).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	4

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DATE: Monday, January 28, 2008

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<u>L32</u>	(nuckolls or sugumar or thimmannagari).in.	237	<u>L32</u>
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<u>L27</u>	l25 and l11	77	<u>L27</u>
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<u>L22</u>	17 and 111	82	<u>L22</u>
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<u>L20</u>	17 and 19	142	<u>L20</u>
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<u>L18</u>	15 and 112	346	<u>L18</u>
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<u>L16</u>	15 and 110	952	<u>L16</u>
<u>L15</u>	15 and 19	952	<u>L15</u>
<u>L14</u>	15 and 18	952	<u>L14</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L13</u>	(711/210-221)[CCLS]	3044	<u>L13</u>
<u>L12</u>	(712/239,240)[CCLS]	739	<u>L12</u>
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<u>L10</u>	(712/2-300)[CCLS]	14119	<u>L10</u>
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<u>L8</u>	(712/2-300)[CCLS]	14119	<u>L8</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L7</u>	15 and L6	201	<u>L7</u>
<u>L6</u>	virtual near12 physical near12 (convert\$3 or conversion\$1 or translat\$5)	6168	<u>L6</u>
<u>L5</u>	(index\$3 or indices or number\$4 or identif\$7 or id or pointer\$3) and 14	1197	<u>L5</u>
<u>L4</u>	11 and 12 and L3	1236	<u>L4</u>
<u>L3</u>	target near5 branch\$4 near5 predict\$5	1682	<u>L3</u>
<u>L2</u>	(entr\$4 or lines\$1) near8 (table or stor\$7 or cach\$3 or tlb)	256075	<u>L2</u>
<u>L1</u>	branch\$5 near15 (predict\$5 or speculat\$5)	7387	<u>L1</u>

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IEEE/IET

Books

Educational Courses

Application Notes [Beta]

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and standards.

- ☐ 1. **Dynamic branch prediction for a VLIW processor**
Hoogerbrugge, J.;
Parallel Architectures and Compilation Techniques. 2000. Proceedings. International Conference on
15-19 Oct. 2000 Page(s):207 - 214
Digital Object Identifier 10.1109/PACT.2000.888345
AbstractPlus | Full Text: PDF(704 KB) IEEE CNF
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- ☐ 2. **Control-flow speculation through value prediction for superscalar processors**
Gonzalez, J.; Gonzalez, A.;
Parallel Architectures and Compilation Techniques. 1999. Proceedings. 1999 International Conference on
12-16 Oct. 1999 Page(s):57 - 65
Digital Object Identifier 10.1109/PACT.1999.807406
AbstractPlus | Full Text: PDF(88 KB) IEEE CNF
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- ☐ 3. **Dynamic hammock predication for non-predicated instruction set architectures**
Klauser, A.; Austin, T.; Grunwald, D.; Calder, B.;
Parallel Architectures and Compilation Techniques. 1998. Proceedings. 1998 International Conference on
12-18 Oct. 1998 Page(s):278 - 285
Digital Object Identifier 10.1109/PACT.1998.727261
AbstractPlus | Full Text: PDF(84 KB) IEEE CNF
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- ☐ 4. **Phaseshift of Electromagnetic Waves Propagating Through Waveguide Junctions (Correspondence)**
Schumacher, D.E.; Ishii, K.;
Microwave Theory and Techniques. IEEE Transactions on
Volume 11, Issue 5, Sep 1963 Page(s):449 - 450
AbstractPlus | Full Text: PDF(248 KB) IEEE JNL
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- ☐ 5. **Incorporating predicate information into branch predictors**
Simon, B.; Calder, B.; Ferrante, J.;
High-Performance Computer Architecture. 2003. HPCA-9 2003. Proceedings. The Ninth International Symposium on
8-12 Feb. 2003 Page(s):53 - 64
Digital Object Identifier 10.1109/HPCA.2003.1183524
AbstractPlus | Full Text: PDF(365 KB) IEEE CNF
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- ☐ 6. **Selective guarded execution using profiling on a dynamically scheduled processor**
Mantripragada, S.; Nicolau, A.;
Innovative Architecture for Future Generation High-Performance Processors and Systems. 1999. International Workshop
1-3 Nov. 1999 Page(s):15 - 22
Digital Object Identifier 10.1109/IWIA.1999.898839
AbstractPlus | Full Text: PDF(640 KB) IEEE CNF

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